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Design and Simulation of Low Power and High Speed Comparator using VLSI Technique

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Abstract: In Digital Wireless Communication application, the design of Low Power and High Speed Analog to Digital Converter (ADC) is the nee d-of- the -day. This paper explores the design of low power and high s pee d comparator us e d in all available ADC architectures. The proposed architecture includes two stage CMOS Operational Amplifier (Op-Amp) circuit. The comparator described here is designed and implemented with 0.18µm technology operate d on 1Volt power supply using Cadence Virtuoso Tool. The functional verification of the comparator is carried out which in turn consumes 0.953 µW of power with propagation delay(s pee d) of 1.561ns. The overall improvement in the results in accordance with the literature is the s cope of this paper.

Keywords: Comparator, Cadence tool, Low power, High Speed, ADC, CMOS.

I. INTRODUCTION

Digital wireless communication applications such as Ultra Wide-Band (UWB) and Wireless Personal Area Network (WPAN) need low-power high-speed ADCs to convert Radio Frequency / Intermediate Frequency signals into digital form for baseband processing. Comparator is an important device widely used in ADC [1].

Comparators are used in ADCs, data transmission, switching power regulators, and many other applications. The comparator design plays a vital role in high speed ADCs. Power consumption & speed are key metrics in comparator design [2]. The comparator is the critical building block for all high speed ADCs, regardless of the architecture, which in large measure determines the overall performance of data converters. It includes the maximum sampling rate, bit resolution, and total power consumption [3].

II. RELATED WORK

Comparators are designed such that for reducing power consumption in the ADC and also to increase speed of the ADC. Various authors have tried for reducing the power consumption and increasing the speed.

For instance S. Kale et. al., have proposed the high speed & low power consumption comparators referred to as an open loop comparators [1].

This comparator is operated with power supply of 2.5V and sinusoidal wave 2.5 V amplitude with 5 kHz frequency & capacitive load which consumes 0.31mW with propagation delay of 3.6ns.

III. COMPARATOR PRINCIPLE

The schematic symbol and basic operation of a voltage comparator are shown in Fig.1 [4], this comparator can be thought of as a decision making circuit. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the positive, Vp, the input of the comparator is at a greater potential than the negative, Vn, input, the output of the comparator is a logic 1, where as if the positive input is at a potential less than the negative input, the output of the comparator is at logic 0.

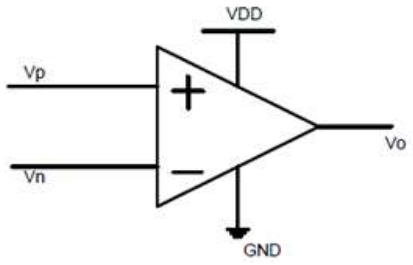

Fig. 1. Basic Comparator

The comparator is widely used in the process of converting analog signals to digital signals. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. In its simplest form, the comparator can be considered as a 1-bit ADC [5]. The presentation on comparators will first examine the requirements and characterization. The comparators can be divided into two types namely, open-loop and regenerative type comparators.

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The open-loop comparators are basically Op-Amps without compensation. Regenerative comparators use positive feedback, similar to sense amplifiers or flip-flops, to accomplish the comparison of the magnitude between two signals. A third type of comparator emerges which is a combination of the both open-loop and regenerative comparators. This combination results in comparators that are extremely fast.

Proposed comparator consists of three stages: the input preamplifier, a latch stage, and an output buffer, depicted in Fig.2.[6]. Preamplifier stage amplifies the input signal t1 improve the comparator sensitivity and isolates the input of the comparator. The latch stage is used to determine which of the input signals is larger and extremely amplifies their difference. The output buffer amplifies the information from latch and outputs a digital signal [7].

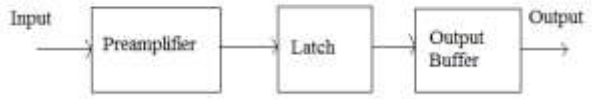

Fig. 2 Comparator Stage

IV. COMPARATOR DESIGN

A comparator acts as the quantizer in the ADCs. Since the comparator is of 1-bit it has only two levels either a „1‟ or a „0‟. A „1‟ implies that VDD = + 1 V and a „0‟ implies that VSS = 0 V. If the input of the comparator is greater than the reference voltage (Vref) it has to give an output of „1‟ and if the comparator input is less than reference voltage then the output of the comparator should be „0‟. A simple comparator performs the required function efficiently.

The reference pulse voltage is supplied in the range of -2.5 V to 1 V. The comparator gives an output voltage of VDD when the input signal is greater than reference voltage and an output of VSS when input signal is less than reference voltage. The Op-Amp can be used as a comparator. The proposed comparator design uses CMOS Op-Amp design technique for achieving high speed & low power consumption [8]. Output buffer is used for stabilizing the output. The proposed CMOS comparator design is as illustrated in Fig. 3.

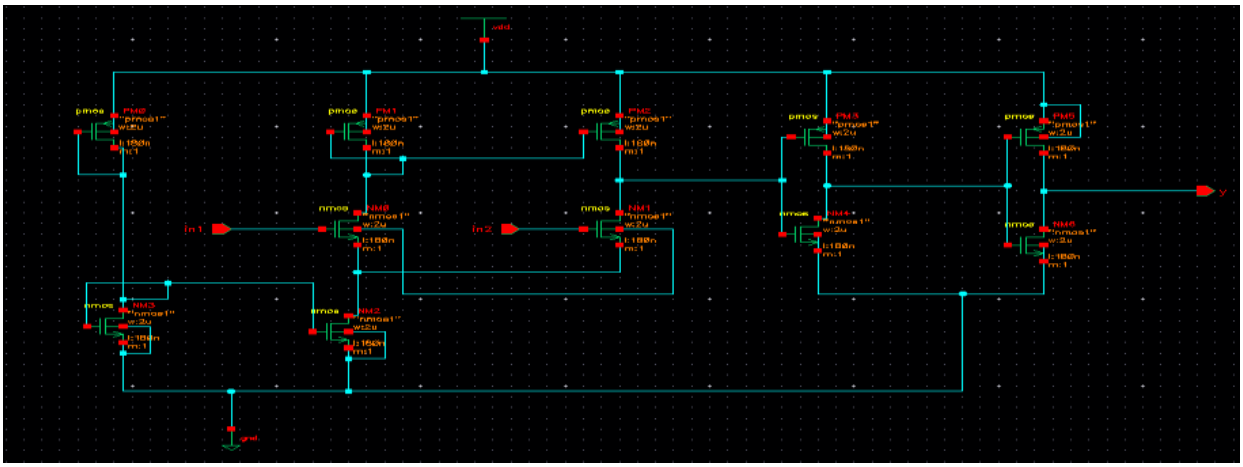

Fig. 3. Proposed Design of a CMOS Comparator

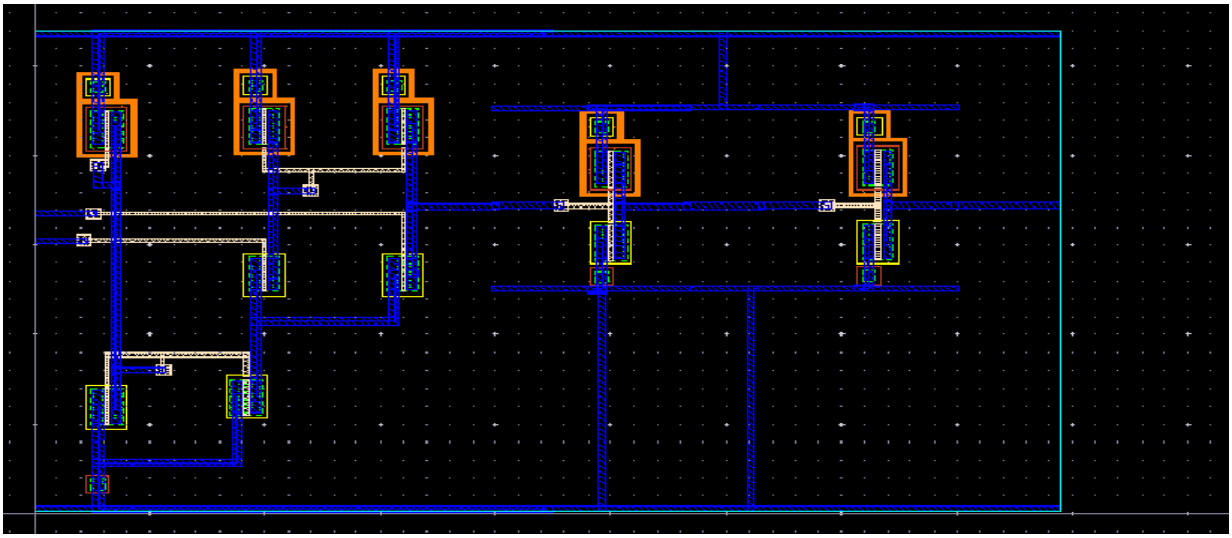

Fig. 4 Layout of Proposed Comparator

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This comparator consists current mirrors, current sinks. Transistor aspect ratios are as selected which in turn gives accurate & optimum results [9].Parasitic effects which influences on the comparators performance is minimized in this design. This helps to get the desired output for a high speed & low power consumption. In this design 1V power supply is used for simulation & designing. This comparator is simulated by using Cadence virtuoso tool with gpdk180 technology library.
The layout of the comparator is as shown in Fig.4.

V. DESIGN ANALYSIS

The most important dynamic parameters that determine the speed of a comparator are the propagation delay and the settling time. The propagation delay is inversely proportional to the input voltage applied. This means that applying a larger input voltage will improve the propagation delay.
The sampling frequency "fsampling" is defined as the reciprocal of the time interval T, as:
Fsampling = 1 / T.
The sampling frequency has to be equal or greater than twice of the frequency bandwidth of analog signals. Dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given by
P = f. C .VDD
Where, f is the output frequency, VDD is the supply voltage, C is the output capacitance.
Clocked, regenerative comparators are fundamental circuit topologies in the field analog- and digital circuit design, which are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback.

VI. SIMULATION RESULTS

The simulation is done using Cadence tool with gpdk180 technology library. We have given sinusoidal wave of 1 V amplitude with 5 kHz frequency on In1 terminal and other terminal is given pulse voltage in range of -2.5 V to 1 V .These inputs are compared by comparator and we have obtained the response as digital (VDD or VSS) as shown in Fig 5. The static power can be measured by applying a static signal (DC) input signal so that no switching occurs. Analo g circuit consumes more power since in their static state many transistors are turned on and consume static power.

Comparators work as a one bit ADCs so the output response of comparator is used to evaluate the binary values for an analog output. Power consumption of this comparator is about 0.953 µW. Power consumption is the most important factor for designing a high performance comparator which will be used in binary search ADC design. Propagation delay of the design is obtained by apply the square wave of 1 V amplitude to In1 terminal of the comparator with In2 terminal is grounded, which is 1.561 nano sec [10]. The design results are shown in Table 1.

TABLE 1.COMPARING DESIGN RESULTS COMPARATOR WITH OTHER COMPARATORS

Performance Parameters	Power Supply	Power Consumption	Propagation delay	Input
Basic Comparator	2 V	34.94 µW	150 µs	2 V
S.Kale.et. al.,	2.5 V	0.31 mW	3.6 ns	2.5 V
Proposed comparator	1 V	0.953 µW	1.561 ns	1 V

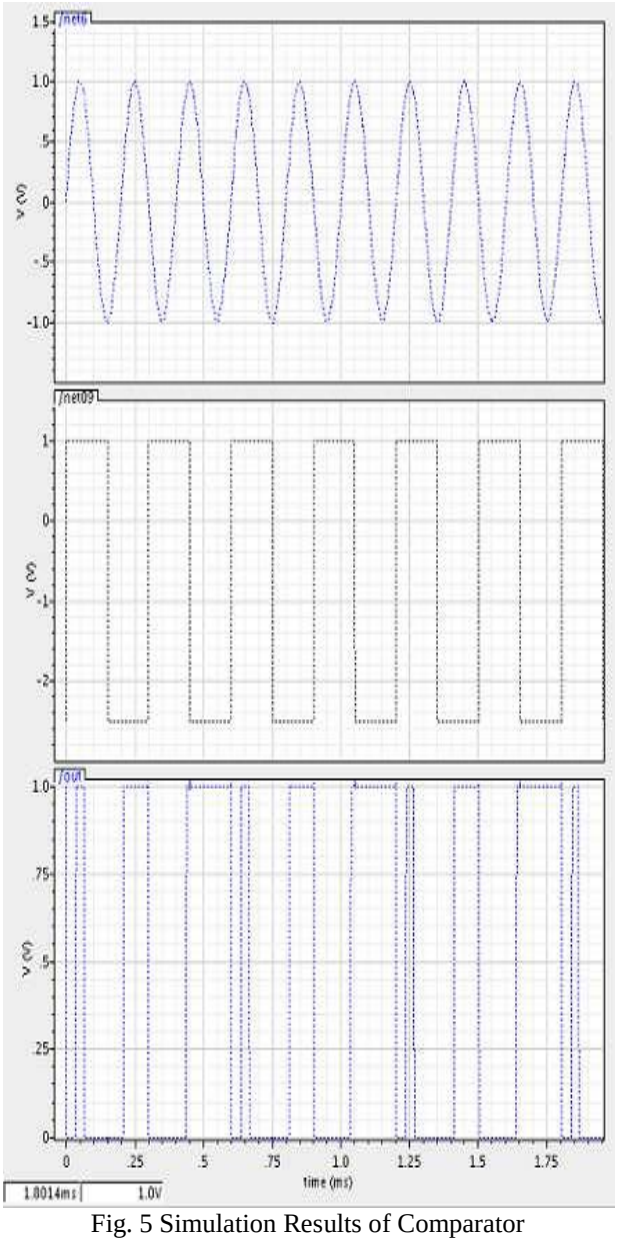

Fig. 5 Simulation Results of Comparator

VII. CONCLUSION

The design, simulation & implementation of CMOS comparator and its performance measurement in terms of

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speed & power is analyzed. The speed of operation of such a comparator is 1 Volt analog with the power consumption of 0.953 µW since it requires 1.561 nano sec and 1 Volt power supply, it finds application in Digital Wireless Communication.

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